

Notice of References Cited	Application/Control No. 10/008,270	Applicant(s)/Patent Under Reexamination CAVANAGH ET AL.	
	Examiner Jason Proctor	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,623,642	04-1997	Katz et al.	703/7
	B	US-6,278,963	08-2001	Cohen, Alain	703/17
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	C.R. Pon, R. Saleh, T. Kwasniewski; "Distributed Circuit Simulation using Waveform Relaxation in a Slotted-Ring Architecture"; Sept. 1994; Electrical and Computer Engineer 1994 Conference Proceedings; pages 545-548 vol. 2
	V	Richard M. Fujimoto, "Parallel and Distributed Discrete Event Simulation: Algorithms and Applications", 1993, Proceedings of the 1993 Winter Simulation Conference, pages 106-114
	W	Jörg Keller, Thomas Rauber, Bernd Rederlechner; "Conservative Circuit Simulation on Shared-Memory Multiprocessors"; 1996; pages 126-134
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.